

REMARKS/ARGUMENTS

Favorable reconsideration of this application as currently amended and in view of the following remarks is respectfully requested.

Claims 1-10 and 16-22 are currently pending. Claims 1, 16, and 17 have been amended by the current amendment.

In the outstanding Office Action, Claims 1, 2, 4, 6, 7, 10, and 16-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,815,374 to Howell in view of U.S. Patent No. 6,218,630 to Takigami; and Claims 1-10 and 16-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,784,262 to Sherman in view of Takigami.

Applicants thank the Examiner for granting an interview on June 23, 2005 to discuss the outstanding prior art issues. During the interview, Applicants' representative and the Examiner discussed proposed claim changes to clarify the location of the via hole of the printed wiring board relative to the semiconductor devices. The amended language found in Claims 1, 16, and 17 is consistent with the language discussed during the interview.

As discussed in the Disclosure of the Invention starting on page 4 of the specification, Applicants have identified a problem regarding wire failure created by a break in a wiring pattern of a printed wiring board where a ball grid array semiconductor chip has been provided. The Applicants discovered that the break was generated during a correction step or an assembly step of the printed wiring board. The present invention addresses the wire failure issue. In particular, the present invention provides a printed wiring board; a semiconductor device including a plurality of first lands formed in a grid and electrically connected to corresponding second lands formed on the printed wiring board. A subset of the second lands correspond to first lands in a corner portion or end portion of the grid. Each second land of the subset includes a primary land and an auxiliary land. Moreover, each of

the subset of second lands connect to a wire provided on the printed wiring board. The primary land includes an arcuate shape and the auxiliary land includes a first portion disposed adjacent the primary land and a second portion connected to the wire wherein the first portion has a greater cross-sectional area than the second portion. Finally, the connecting wire for each land of the subset of second lands includes a via land, and the via land includes an arcuate portion electrically connected to a via hole formed in the printed wiring board outside of the footprint of the grid of the semiconductor device.

As pointed out to the Examiner during the interview, Howell illustrates in Figure 13 a via hole provided below semiconductor device 66. Consequently, Howell does not address the problems discovered by the Applicant or provide the solution regarding wire failure of a printed wiring board caused by warpage and distortion during the soldering step or during an assembling step.

Likewise, Takigami fails to teach or suggest a connecting wire for each land of a subset of lands which is connected to a via hole formed in the printed wiring board outside of the footprint of the semiconductor device. Consequently, Takigami does not address the problem discovered by the Applicants or provide the claimed solution.

Finally, Sherman much like Howell teaches that the throughholes 22A are provided beneath semiconductor device 12. Consequently, Sherman does not address the deficiencies of Howell.

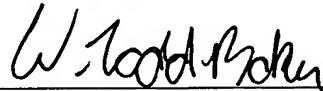
For the foregoing reasons, Howell is not believed to anticipate or render obvious the subject matter defined by the pending claims when considered alone or in combination with Takigami or Sherman.

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Consequently, no further issues are believed to be outstanding, and the application is believed to be in condition for allowance. An early and favorable action is therefore respectfully requested.

Respectfully submitted,

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